UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/651,944	08/31/00	DRAPKIN O.	ATI-000152BT

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MM91/1108

EXAMINER	
NGUYEN, H	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED:
11/08/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No.	Applicant(s)	
	09/651,944	DRAPKIN ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 18-25* is/are rejected.

7)☒ Claim(s) *16 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitation "an output device" on line 1-2 of claim 2 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Objection

Claims 19 and 23 are objected to because the recitation " said introducing step" on line 2 lacks antecedent basis.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 3, 7, 8, 9,10, 19 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 2, the recitation "an input/output device' on lines 1-2 is indefinite because it is misdescriptive. It can be seen from figures 1-4, none of the disclosed circuit proves that it is an input/output device i.e., it can transmit and receive signal. The same analysis is true for claims 7 and 10.

Regarding claim 3, the recitation "preventing discharge" on line 4 is indefinite because it is unclear what part of the circuit it can be prevented from being discharged into.

Regarding claim 8, the recitation "for compensating for preventing current from" on lines 5-6 is indefinite because it is unclear what it is meant by.

Claims 9, 19 and 20 are rendered indefinite by the deficiencies of claims 2, 3 and 8.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-15 and 18-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishikawa et al. (Japanese Pat. JP02000252430A).

Regarding claim 1, figure 2 of Ishikawa shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance, comprising the step of:

detecting a direction of change of the input voltage (high or low) at input (1);

introducing a current when transistor (2) is turned on with a positive edge of the input signal to charge the parasitic capacitance (4) to compensate the current of the input signal.

Regarding claim 2, the circuit of figure 2 shows a circuit of an input/output device.

Regarding claim 3, transistor (2) is turned off in response to a negative edge of the input and capacitor (4) is discharge via element (5), thus preventing discharging of parasitic capacitance (4) into the input signal.

Regarding claim 4, similar to the method of claim 1, the impedance of the parallel circuit (5) change when transistor (2) is turned on in response to a positive edge of the input signal to reduce distortion of the input signal.

Regarding claim 5, figure 2 of Ishikawa shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (2) for detecting changes of the input voltage; a correction circuit (5) coupled to the detection circuit for compensating the current from the input signal diverted to the parasitic capacitance due to the positive edge of the input signal.

Regarding claim 6, the detection circuit (2) inherently includes a capacitance (gate – source capacitance).

Regarding claim 7, the circuit of figure (2) is an input/output device.

Regarding claim 8, figure 2 of Ishikawa shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (2) for detecting the change of the input signal and a correction circuit (5) for preventing current from the parasitic capacitance (4) to be added to the input signal due to a negative edge of the input signal. Note that capacitance (4) discharges through (5) when transistor (2) is turned off. The detection circuit includes a capacitance (3) and the circuit of figure (2) is an input/output device.

Regarding claim 9, the detection circuit includes capacitance (3).

Regarding claim 10, the circuit of figure (2) is an input/output device

Regarding claim 11, the claim circuit is identical to the circuit of claim 4 and it is read in figure 2 of Ishikawa.

Regarding claim 12, the claim circuit is identical to the circuit of claim 1 and it is read in figure 2 of Ishikawa.

Regarding claim 13, the claim circuit is identical to the circuit of claim 3 and it is read in figure 2 of Ishikawa.

Regarding claim 14, figure 2 of Ishikawa shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a first element (5), a second circuit element (3) blocking the discharge of the parasitic capacitance and a control circuit (2). Note that the second circuit (3) is "turned off" when a positive voltage from the control circuit (2) applies to its negative terminal and circuit (3) is turned on when circuit (2) does not conducts due to a negative going edge input signal is applied to the input (1).

Regarding claim 15, first and second circuit elements (5, 3) have a common terminal coupled to the parasitic capacitor (4).

Regarding claim 18, the parasitic capacitance (4) is across the input (1) and ground.

Regarding claim 19, the parasitic capacitance (4) is across the input (1) and ground. Element (5) introduces a current to the input.

Regarding claim 20, the parasitic capacitance (4) appears between the input (1) and ground.

Regarding claim 21, the parasitic capacitance (4) appears between the input (1) and ground.

Regarding claim 22, the parasitic capacitance (4) appears between the input (1) and ground.

Regarding claim 23, the parasitic capacitance (4) appears between the input (1) and ground. Element (5) introduces a current to the input.

Regarding claim 24, the parasitic capacitance (4) appears between the input (1) and ground. Element (5) introduces a current to the input .

Regarding claim 25, the detection circuit (2) inherently has a capacitance (gate-source or gate-drain capacitance) that is connected to one terminal of the parasitic capacitance (4).

Claims 1-3, 5, 7, 8, 10-13 and 18-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Bruccoleri et al. (US Pat. 5,808,488).

Regarding claim 1, figure 3 of Bruccoleri shows a method for reducing distortion of a signal to and input of an input/output device having parasitic capacitance, comprising the step of:

detecting a direction of change of the input voltage (high or low) at input (I+);

introducing a current when INV2 has high level output with a positive edge of the input signal to charge the parasitic capacitance (Cin) to compensate the current of the input signal.

Regarding claim 2, the circuit of figure 3 shows a circuit of an input/output device.

Regarding claims 3, INV1 detects a direction of change in voltage of the input signal, INV2 has low output level in response to a negative edge input signal, the parasitic capacitance discharges though INV2, thus preventing discharging of the parasitic capacitance into the input signal.

Regarding claim 5, figure 3 of Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (INV1) for detecting changes of the input voltage; a correction circuit (INV2) coupled to the detection circuit for compensating the current from the input signal diverted to the parasitic capacitance due to the positive edge of the input signal.

Regarding claim 7, circuit of figure 3 is an input/output device.

Regarding claim 8, figure 3 of Bruccoleri shows an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a detection circuit (INV1) for detecting the change of the input signal and a correction circuit (INV2) for preventing current from the parasitic capacitance (Cin) to be added

to the input signal due to a negative edge of the input signal. Note that capacitance (Cin) discharge through a transistor of (INV2) due to a negative edge of the input signal.

Regarding claim 10, circuit of figure 3 is an input/output device.

Regarding claim 11, the claim circuit is identical to the circuit of claim 4 and it is read in figure 3 of Bruccoleri.

Regarding claim 12, the claim circuit is identical to the circuit of claim 1 and it is read in figure 3 of Bruccoleri.

Regarding claim 13, the claim circuit is identical to the circuit of claim 3 and it is read in figure 3 of Bruccoleri.

Regarding claim 18, parasitic capacitance (Cin) is across the input and ground. And it introduces current to the input when (INV2) is at high level.

Regarding claim 19, parasitic capacitance (Cin) is across the input and ground. And it introduces current to the input when (INV2) is at high level.

Regarding claims 20-22 and 24, the parasitic capacitance (Cin) is across the input and ground.

Regarding claim 23, parasitic capacitance (Cin) is across the input and ground. And it introduces current to the input when (INV2) is at high level.

Allowable Subject Matter

Claims 16 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 16 and 17 are objected to because the prior art of record fails to teach or fairly suggest an apparatus for an apparatus for reducing distortion of a signal applied to an input of a circuit at high frequency a having parasitic capacitance, comprising: a first element for providing current to the parasitic capacitance, a second circuit element for monitoring the input signal and a control circuit monitoring the input signal wherein, first and second circuit elements are PMOS and NMOS transistors as called for in claims 16 and 17.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
Examiner
11-05-01

MY-TRANG NU TON
PRIMARY EXAMINER